



产品规格承认书

Product Specifications for Approval

日欣型号(NISIN Model): NS120AM1301AZ01

客户名称(Customer) : _____

客户型号(Customer Model):		
Approved by Customer		
结构(Mechanica)	电子(Electronic)	项目 (PM)

日欣光电 (NISIN Optoelectronics)		
Designed	Checked	Approved



修改记录

日期	版本	修改内容	页数	拟制
2026-09-18	V00	初版发行	所有	李世龙

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1.产品规格（Product Specifications）

面板类型（Panel Type）	AMOLED
面板尺寸 (Panel Size)	1.2 inch
总成尺寸（Panel outline）	35*35*1.54mm
分辨率（Resolution）	390 *(RGB) * 390
显示点间距（Dot Pitch）	0.078* 0.078mm
显示色彩（color）	16.7M
视角（View Angle）	All direction
帧率（Frame rate）	60Hz
每英寸像素数（Pixel Per inch）	459.62
模组（LCM Outline）	33.22*33.75*0.67mm
显示区（Active Area）	30.420*30.420mm
显示驱动 IC（Display Driver IC）	C05300
接口类型（Interface Type）	QSPI
总成亮度（LCM Brightness）	Typ:600cd/m2



3. 接口定义（The Interface Definition）

AMOLED Pin No.	Symbol	I/O	Function
1	MTP	Power	MTP programming power supply pin. (8.25V typical) - Must be left open or connected to VSSD in normal condition.
2	VBAT	Power	Power supply for Power IC , Voltage Range 2.9~5.5V.
3	SDA0	I/O	data signals if QSPI interface.
4	SDA1	I/O	data signals if QSPI interface.
5	SDA2	I/O	data signals if QSPI interface.
6	SDA3	I/O	data signals if QSPI interface.
7	CS	Power	Chip select input pin ("Low" enable) in QSPI I/F.
8	SCL	Power	A synchronous clock signal in QSPI I/F.
9	TE	Digital Output (VDDI-VSSI)	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is output low.
10	RST	Power	Ground.
11	IOVCC	Power	Power supply for display driver IC interface and logic system.
12	VCC	Power	Power supply for Power IC Enable
13	GND	Power	Ground.

4. 电性特性（Electrical Characteristics）

4.1. Absolute Maximum Ratings

Absolute Maximum Ratings List

Item	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Power supply voltage	VDDI ~ VSSD	-0.3	-	+5.5	V
Power supply voltage	VCI (VCIA, VCIC, VCIR) ~ VSSA	-0.3	-	+5.5	V
Supply voltage	AVDD ~ VSSA	-0.3	-	+6.6	V
Supply voltage	AVSS ~ VCL	-0.3	-	+5.0	V
Supply voltage	VGH ~ VGL	VGH-VGL ≤ 30			V
Operating temperature	Topr	-40		+85	°C
Storage temperature	Tstg	-55		+125	°C
Input voltage	Vin	-0.3		VDDI+0.3	V

4. 2. DC Characteristics

DC Characteristics List

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Notes
Power generation & Operation Voltage							
AVDD booster voltage	AVDD	Operating Voltage	4.5	-	6.5	V	
VCL booster voltage	VCL	Operating Voltage	-5.0	-	-3.5	V	
Analog Operating voltage	VREFP	Operating Voltage	0.5	-	5.0	V	
Analog Operating voltage	VREFN	Operating Voltage	-5.0	-	-0.5	V	
Analog Operating voltage	I_ELVD	Operating Voltage	2.0	-	5.0	V	
Analog Operating voltage	I_ELVS	Operating Voltage	-5	-	-0.5	V	
Gamma reference voltage	VGMP	Operating Voltage	2	-	6.3	V	
Gamma reference voltage	VGSP	Operating Voltage	0	-	4.5	V	
VGH booster voltage	VGH	Operating Voltage	3	-	10.6	V	
VGL booster voltage	VGL	Operating Voltage	-15	-	-2	V	
Voltage difference between VGH and VGL	VGH-VGL	$ VGH-VGL \leq 30$			30	V	
I/O operating voltage	VDDI	I/O supply voltage	1.65	-	3.3	V	
LOGIC INPUT/ OUTPUT							
Logic High level input voltage	V _{IH}		$0.8 \times VDDI$	-	VDDI	V	1
Logic Low level input voltage	V _{IL}	-	VSS	-	$0.2 \times VDDI$	V	1
Logic High level output voltage	V _{OH}	I _{OH} = -0.1mA	$0.8 \times VDDI$	-	VDDI	V	2
Logic Low level output voltage	V _{OL}	I _{OL} = +0.1mA	VSS	-	$0.2 \times VDDI$	V	2
Logic High level leakage	ILIH1	V _{in} = 0 to VDDI	-	-	1	μA	1,2
Logic Low level leakage	ILIL1	V _{in} = 0 to VDDI	-1	-	-	μA	1,2
Source OP Output							
Output deviation voltage	V _{dev}	S _{out} ≥ 4.2V S _{out} ≤ 0.8V			TBD	mV	
Output deviation voltage	V _{dev}	4.2V > S _{out} > 0.8V			TBD	mV	
Output offset voltage	V _{OFSET}				TBD	mv	
Stand-by Current							
Sleep In mode	I _{stip1}	DSI LP mode VDDI Current		110		μA	
		DSI LP mode VCI Current		25		μA	1
	I _{stul1}	DSI Ultra Low power VDDI Current		85		μA	
		DSI Ultra Low power VCI Current		25		μA	1
Deep Stand-by mode	I _{DSTB}	VDDI Current		2		μA	
		VCI Current		1		μA	1

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Notes
Oscillator Output							
Oscillator tolerance	Δ OSC	All Temperature	-2%	-	2%	%	3

Note 1: Including of all logic I/O pins.
Note 2: Including of TE, TE1, SWIRE, OLED_EN.
Note 3: Oscillator = 22MHz.

4.3.Timing Characteristics

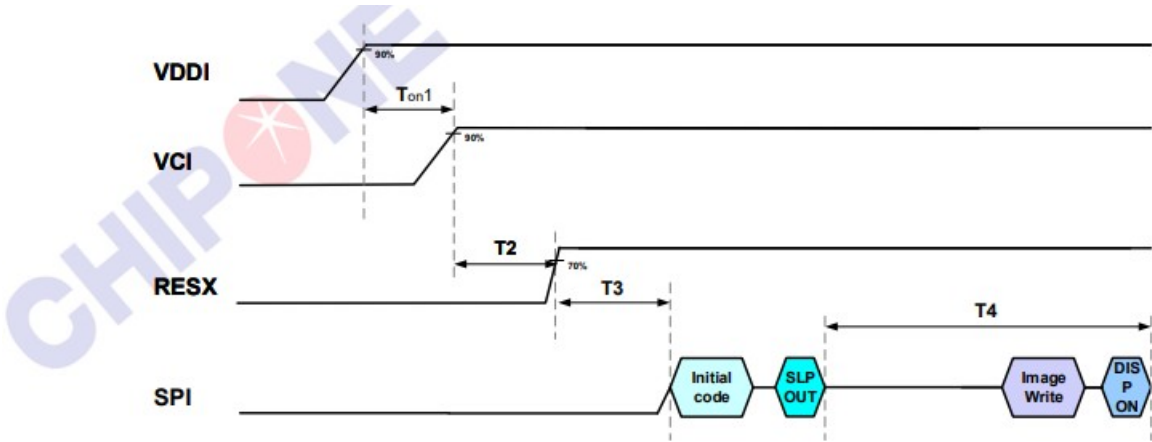
4.3.1.Display panel Power on /off sequence

The power on sequence for different power input modes are shown below figures.

Power ON Sequence Timing

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
T _{on1}	VDDI on to VCI on delay	>0			us	
T ₂	VDDI on to valid to RESET high	10			ms	
T ₃	RESET high to first command	10			ms	
T ₄	Sleep-out command received to Display on command received.	60			ms	

The Power on sequence is shown as below.



SPI Power ON Sequence

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.
Note 2: This power-on sequence is based on adding Schottky diode on VGL pin to ground.

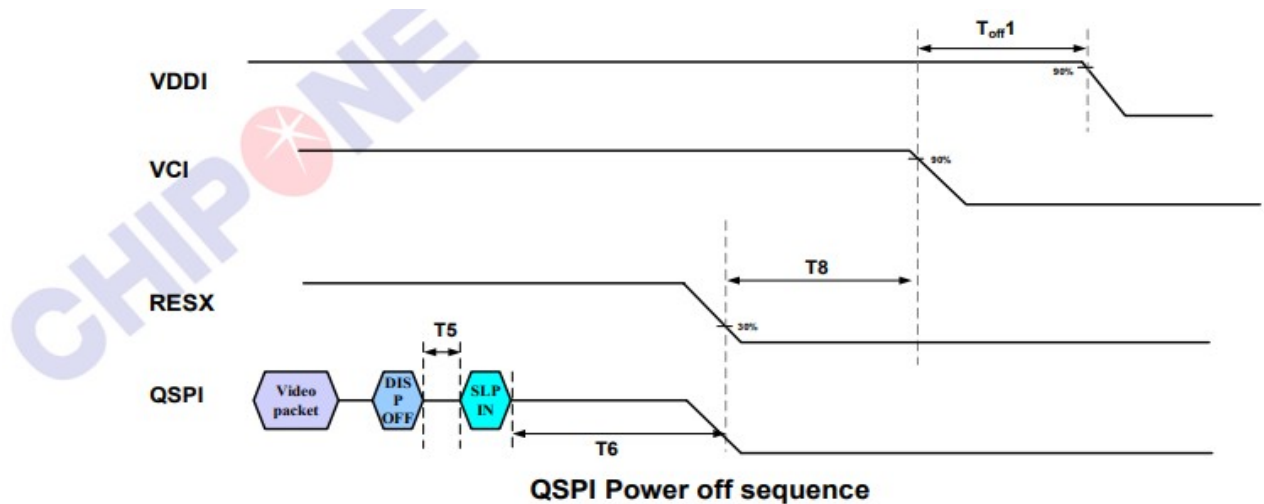
Power OFF Sequence

The power off sequence for different power input modes are shown below figures.

Power OFF Sequence Timing

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
T _{off1}	VCI off to VDDI off delay	>0			us	
T5	Display-off command received to Sleep-in command delay	>0			us	
T6	Sleep-in command received to valid to RESET low	83			ms	@60Hz
T7	MIPI ultra low power mode to valid to RESET low	0			us	
T8	RESET low to VCI off delay	0			us	

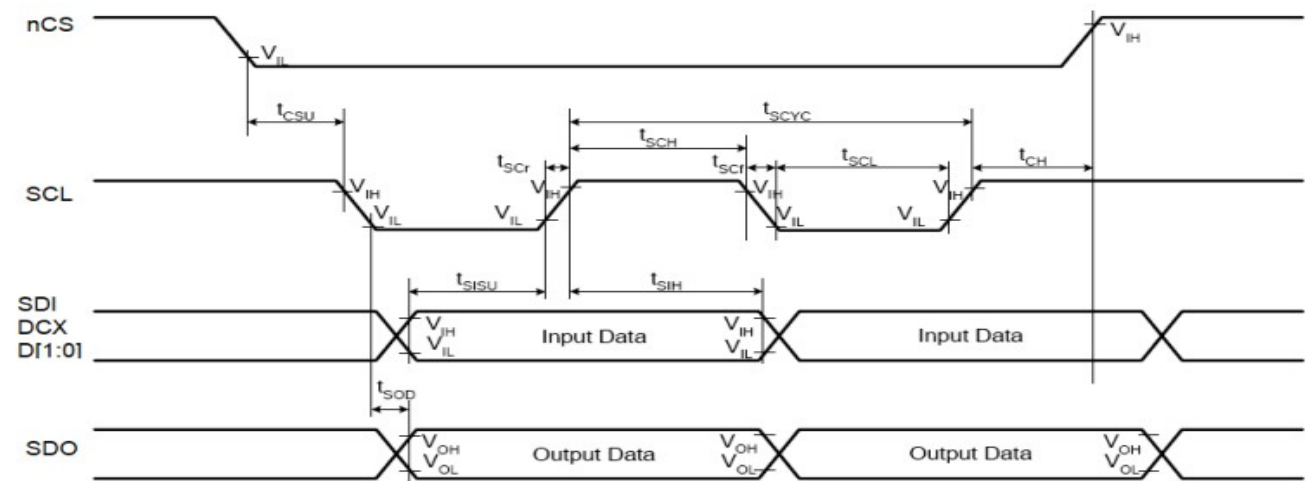
The power off sequence is shown as below:



- Note 1:** Unless otherwise specified, timings herein show cross point at 50% of signal/power level.
- Note 2:** Keep VGH is equal to or larger than VCI during power off sequence.

4. 3. 2. AC Timings Characteristics

Serial Interface Characteristics (QUAD SPI)



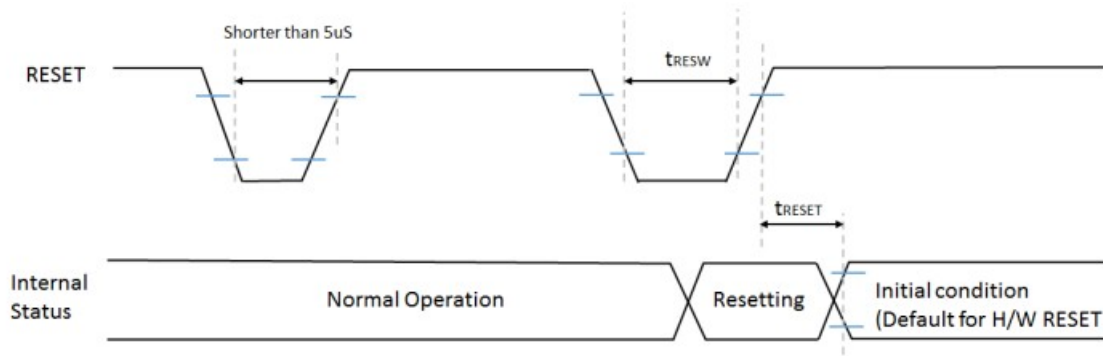
Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
SCL	T _{SCYC}	Clock cycle (Write)	20	-	-	ns	
	T _{SCYC}	Clock cycle (Read)	100	-	-	ns	
	T _{SCH}	Clock "H" pulse width (Write)	6.5	-	-	ns	
	T _{SCH}	Clock "H" pulse width (Read)	45	-	-	ns	
	T _{SCL}	Clock "L" pulse width (Write)	6.5	-	-	ns	
	T _{SCL}	Clock "L" pulse width (Read)	45	-	-	ns	
	T _{Scr}	Clock rise time	-	-	3.5	ns	
	T _{Srf}	Clock fall time	-	-	3.5	ns	
CSX	T _{CSU}	Chip select setup time	10	-	-	ns	
	T _{CH}	Chip select hold time	10	-	-	ns	
SDI DCX D[1:0]	T _{SISU}	Data input setup time	4	-	-	ns	
	T _{SIH}	Data input hold time	4	-	-	ns	
SDO	T _{SOD}	Data output setup time	-	-	45	ns	
	T _{SOH}	Data output hold time	5	-	-	ns	

Note 1: Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

Note 2: Ta = -30 to 85 °C, VDDI=1.65V to 3.3V, VCI=2.7V to 3.6V, GND=0V

Note 3: The max SCL sequence of 4-wire QSPI transferring RGB888, RGB666 and RGB555 is 50Mhz.

4.3.3. Display panel reset timing:



Reset Input Timing

Signal	Symbol	Parameter	Description	Specification			Unit	Notes
				MIN	TYP	MAX		
RESET	tRESW	Reset "L" pulse width		10			µS	1
	tRESET	Reset complete time	When reset applied during Sleep in mode			5	mS	2
			When reset applied during Sleep Out mode			120	mS	5

Note 1: Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table below.

Reset Input Actions

RESET Pulse	Action
Short than 5us	Reset Rejected
Long than 10μS	Reset
Between 5us and 10μS	Reset Start

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.

Note3: During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time(t_{RESET}) within 5ms after a rising edge of RESET.

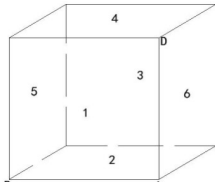
Note4: Spike Rejection also applies during a valid reset pulse as shown below.



Note5: It is necessary to wait 5ms after releasing RESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

5.可靠性实验测试(Reliability Test Conditions And Methods)

序号	试验项目	试验条件及方法	试验设备	检验项目	检验工具
1	高温高湿(静、动态)试验	温度 60℃ ± 3℃, 湿度 90% ± 3%, 要求选择时间分别为 96 小时, 静、动态 (产品点亮) 在室温下恢复 2 小时后进行外观, 显示功能全画面检查。	恒温恒湿试验机	检验外观、功能、抗腐蚀性	目视/测试架/客户样机/显微镜
2	高、低温冲击试验	静态-30℃ (30 分钟) ∞ 80℃ (30 分钟) ∞ -30℃ (30 分钟), 24 个循环, 在室温下恢复 2 小时后进行外观, 显示功能全画面检查。	冷热冲击试验机	检验外观、功能	
3	高温贮存试验	常温 70℃ ± 3℃、宽温 80℃ ± 3℃、96 小时后在室温状态下恢复 1 小时在 2 小时内完成外观、显示功能全画面检查。	烤箱	检验外观、功能	目视/测试架/客户样机
4	低温贮存试验	常温 -20℃ ± 3℃、宽温 -30℃ ± 3℃、条件的试验箱内保存 96 小时后在室温状态下恢复 1 小时, 在 2 小时完成外观、显示功能全画面检查, 特别注意检查是否有漏液、断线、腐蚀、偏光片不良现象。	低温冰箱	检验外观、功能	
5	低温贮存试验(动态)	常温 -20℃ ± 3℃、宽温 -30℃ ± 3℃ 条件的试验箱内点亮刷屏, 过程中每 1 小时观察一次, 全画面检查显示功能如: 异常, 卡机, 花屏等。特别注意检查是否有漏液、断线、腐蚀、偏光片不良现象。	低温冰箱	检验外观、功能	目视/测试架/客户样机

6	包 装 模 组 跌 落 试 验	1、跌落重量及自由落体高度： (图二) / <table><tr><th>总重量</th><th>自由落体高度</th></tr><tr><td>0-9kg</td><td>92cm</td></tr><tr><td>9-25kg</td><td>76cm</td></tr><tr><td>25-45kg</td><td>53cm</td></tr><tr><td>45-68kg</td><td>46cm</td></tr><tr><td>大于 68kg</td><td>41cm</td></tr><tr><td></td><td></td></tr></table>  2、自由落体角度如下： 1) 一角：A 角 2) 三菱：A-B, A-D, A-C 3) 六面：面 1, 面 2, 面 3, 面 4, 面 5, 面 6;	总重量	自由落体高度	0-9kg	92cm	9-25kg	76cm	25-45kg	53cm	45-68kg	46cm	大于 68kg	41cm			包装模组跌落架	测试电性能无异常、外观检验无破损，无脱离现象	目视/测试架/客户样机
总重量	自由落体高度																		
0-9kg	92cm																		
9-25kg	76cm																		
25-45kg	53cm																		
45-68kg	46cm																		
大于 68kg	41cm																		
7	盐 雾 试 验	标准条件:中性盐雾试验 (NSS 试验)：5%的氯化钠盐水溶液, 溶液 PH 值中性 (6.5~7.2)，试验温度 35±2℃，盐雾的沉降率在 1~2ml/80cm².h 之间, 时间 24h。2. 其它特殊要求条件:醋酸盐雾试验 (ASS 试验)：5%氯化钠溶液中配入冰醋酸, 溶液 PH 值为 3 左右, 试验温度 35±2℃，盐雾的沉降率在 1~2ml/80cm².h 之间, 时间 24h。全画面检查外观、功能，特别注意检查是否有腐蚀	盐雾试验设备	检验外观、功能，盐雾试验结果的判定方法，腐蚀物出现判定法: 定性判定，试验后功能测试应 OK，外观观察产品无腐蚀现象产生。	目视/测试架/客户样机/显微镜														
8	ESD 抗 静 电 试 验	1) 装整机状态下试验:接触 4KV, 非接触 8KV 放电测试, 接触测试时, LCM 通电状态下测 5 个点。 2) 测试架测试状态下试验: 接触 4KV, 非接触 8KV 放电测试, 接触测试时, LCM (或总成) 通电状态下测 9 个点。其中产品正面显示区域两个点, 产品显示区域背面 4 个点, 产品左侧面、右侧面和 IC 端对面中间位置各一个点。(如 6.17.3.3 图所示) 测试点 1—6 是空气放电, 测试点 7—9 是接触放电, 10 次/点。总成 (或模组) 实验后在图案、黑色、白色、灰阶画面各撕膜 3~5 次, 确认有无撕膜静电不良, 撕膜静电速度适中, 不可过快及刻意放慢。判定标准: 撕膜 3 次确认无撕膜静电 , OK。撕膜 3 次以上出现撕膜静电, 在保护膜覆盖后 3 秒内静电消失 OK。撕膜出现撕膜静电, 在保护膜覆盖后 3 秒内静电不消失 NG。	抗 静 电 枪 (尖头接触放电, 圆头空气放电)	检验外观、功能	目视/测试架														

6. 光电参数（Optical Characteristics）

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Surface Luminance	Lv	$\theta=0^\circ$ $\phi=0^\circ$ $T_a=25^\circ\text{C}$	-	350	-	cd/m ²	Note1
Luminance uniformity	δ WHITE		85	-	-	%	Note2
Contrast Ratio	Cr		30000	-	-	-	Note3
Viewing Angle	θ	Up/Down/ Right/Left $Cr \geq 10$	88	-	-	deg	Note4
Color Coordinate of CIE1931	Red x	$\theta=0^\circ$ $\phi=0^\circ$ $T_a=25^\circ\text{C}$	0.657	0.687	0.717	-	Note 5
	Red y		0.282	0.312	0.342		
	Green x		0.185	0.225	0.265		
	Green y		0.692	0.732	0.772		
	Blue x		0.107	0.137	0.167		
	Blue y		0.023	0.053	0.083		
	White x		-	0.300	-		
	White y		-	0.310	-		
NTSC ratio	-	-	90	110	-	%	CIE1931
Life Time	T95	25 $^\circ\text{C}$	240	-	-	hours	-

Note:

All of the data above are based on module with POL, and the transmittance of POL is 42%.

Note1. Surface Luminance

- Measurement equipment: CS2000 or similar equipment.
- Measuring surroundings: Dark room.
- Measuring temperature: $T_a=25^\circ\text{C}$.
- The data are measured after OLEDs are lighted on for more than 5 minutes and all pixels are fully white.
- The Surface Luminance is the average value of 5 measured spots (Fig-1):
 $L_v = \text{Average Luminance with all white pixels (P}_1, P_2, P_3, P_4, P_5)$

Note2. Luminance Uniformity

- Measurement equipment: CS2000 or similar equipment.
- Measuring surroundings: Dark room.
- Measuring temperature: $T_a=25^\circ\text{C}$.
- The data are measured after OLEDs are lighted on for more than 5 minutes and all pixels are fully white.
- The Luminance Uniformity is calculated by using following formula:
 $\delta \text{ WHITE} = L_p (\text{Min.}) / L_p (\text{Max.}) \times 100 (\%)$
 $L_p (\text{Min.}) = \text{Minimum Luminance with all white pixels (P}_1, P_2, P_3, P_4, P_5)$
 $L_p (\text{Max.}) = \text{Maximum Luminance with all white pixels ((P}_1, P_2, P_3, P_4, P_5)$

Note3. Contrast Ratio

- Measurement equipment: CS2000 or similar equipment.
- Measuring surroundings: Dark room.
- Measuring temperature: $T_a=25^\circ\text{C}$.
- The data are measured after OLEDs are lighted on for more than 5 minutes.
- The Contrast Ratio is calculated by using following formula:

Contrast Ratio(Cr) = L_w / L_b

L_w = Average Luminance with all **white** pixels (P_1, P_2, P_3, P_4, P_5)

L_b = Average Luminance with all **black** pixels (P_1, P_2, P_3, P_4, P_5)

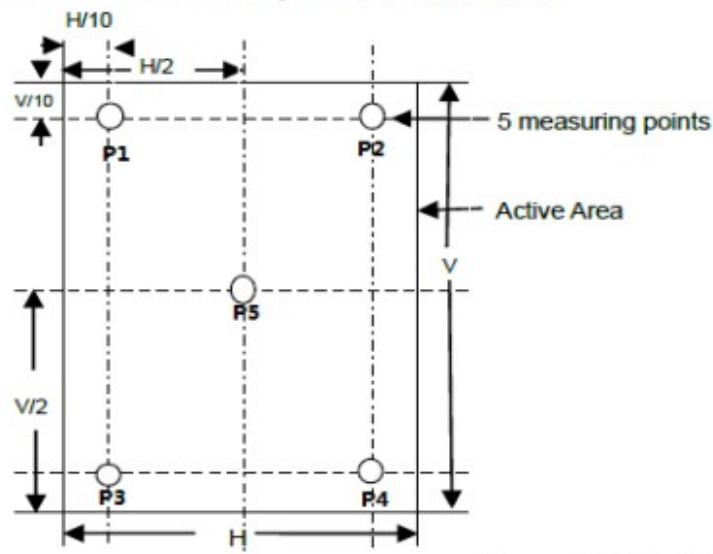


Fig-1

Note4. Viewing Angle

- Measurement equipment: DMS803 or similar equipment.
- Measuring surroundings: Dark room.
- Measuring temperature: $T_a=25^\circ\text{C}$.
- The Viewing Angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the display surface.

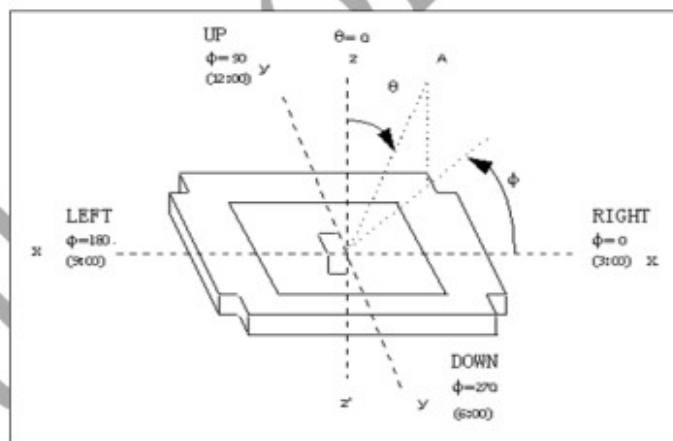


Fig-2

Note5. Color Coordinate of CIE1931

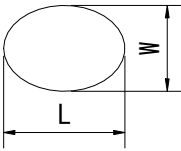
- Measurement equipment: CS2000 or similar equipment.
- Measuring surroundings: Dark room.
- Measuring temperature: $T_a=25^\circ\text{C}$.
- The x, y value of Color Coordinate is determined by measuring at center position of the display panel.

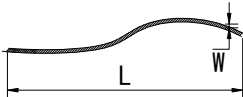
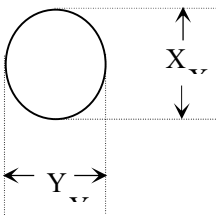
■ RELIABILITY TEST

No.	Test Item	Test Condition	Qty	Inspection after test
1	High Temperature Storage	80℃ ±2℃/120 hours	5	Inspection after 2 hours storage at room temperature, the sample shall be free from defects: 1. Remarkable deterioration of No clearly visible defects or display quality. However, any polarizer's deteriorations by the high temperature/ High humidity Storage test and the High temperature/ High humidity Operation test are permitted. 2. No function-related abnormalities. 3. Optical criteria : White Δu*v' ≤0.02 4. No visible defects .(optical / mechanical) .
2	Low Temperature Storage	-30℃ ±2℃/120 hours	5	
3	High Temperature Operating	70℃ ±2℃/120 hours	5	
4	Low Temperature Operating	-20℃ ±2℃/120 hours	5	
5	Temperature Cycle storage	-30 ℃ ±2 ℃ ~25~80 ℃ ±2 ℃ ×10cycles (30min.) (5min.) (30min.)	5	
6	High Temperature Humidity Storage	60℃ ±5℃ ×90%RH/120 hours	5	
Remark: 1.The test samples should be applied to only one test item. 2.For Damp Proof Test, Pure water(Resistance> 10MΩ) should be used. 3.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part. 4.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.				

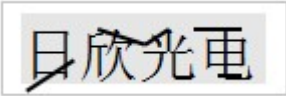
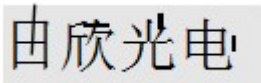
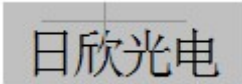
7.检验标准 (Inspection standard)

7.1、外观检验标准:

项目	不良描述	判定标准			检验方法
1-1 外观 (次缺)	产品外观或点亮状态下的圆形物 (LCD/POL/BL/盖板/TP/组装异物/贴合异物、产品本身的亮点/暗点等)  $\Phi=(L+W)/2$	> 2.4 寸——7.0 寸			目视 (菲林卡比对)
		点状直径	允许个数	备注	
		$\Phi \leq 0.10\text{mm}$	不计	1: 10mm 间距内只允许 3 个点。 2: 显示区只允许 10 个点, 超过以上任意一项则 NG	
		$0.1\text{mm} < \Phi \leq 0.15\text{mm}$	4	TP、屏各允许 2 个	
		$0.15\text{mm} < \Phi \leq 0.2\text{mm}$	2	TP、屏各允许 1 个	
		$\Phi > 0.2\text{mm}$	0		

1-2 外观 (次 缺)	产品外观或点亮状态下的 的线状物 (LCD/POL/BL/ 盖板/TP/组装异物/贴合 异物、产品本身的亮点/ 暗点等) 	<table><tr><td>长 (L)</td><td>宽 (W)</td><td>允许 个数</td></tr><tr><td>≤1mm</td><td>≤0.03mm</td><td>2</td></tr><tr><td>≤2mm</td><td>0.03<W≤0.05mm</td><td>1</td></tr><tr><td>>2mm</td><td>>0.05mm</td><td>NG</td></tr></table> 注意：两条线之间必须距离 10mm 以上（>2.4 寸—7.0 寸）。	长 (L)	宽 (W)	允许 个数	≤1mm	≤0.03mm	2	≤2mm	0.03<W≤0.05mm	1	>2mm	>0.05mm	NG	目视 (菲 林卡 比对)
长 (L)	宽 (W)	允许 个数													
≤1mm	≤0.03mm	2													
≤2mm	0.03<W≤0.05mm	1													
>2mm	>0.05mm	NG													
1-3 外观 (次 缺)	气泡： Φ= (X+Y) /2 	<table><tr><td>尺寸</td><td>允许个数</td></tr><tr><td>1、Φ ≤0.1mm 2、不超过边框 1/3</td><td>不计 (密集不可)</td></tr><tr><td>0.10<Φ ≤0.2mm</td><td>1</td></tr><tr><td>Φ >0.2mm</td><td>NG</td></tr><tr><td>0.2<Φ ≤1.5mm, (边框以外)</td><td>3</td></tr></table> 注意：>2.4 寸-6.0 寸气泡间距大于 10mm 以上	尺寸	允许个数	1、Φ ≤0.1mm 2、不超过边框 1/3	不计 (密集不可)	0.10<Φ ≤0.2mm	1	Φ >0.2mm	NG	0.2<Φ ≤1.5mm, (边框以外)	3	在日 光台 灯下 撕起 保护 膜, 距 待测 物 30cm 目视		
尺寸	允许个数														
1、Φ ≤0.1mm 2、不超过边框 1/3	不计 (密集不可)														
0.10<Φ ≤0.2mm	1														
Φ >0.2mm	NG														
0.2<Φ ≤1.5mm, (边框以外)	3														
1-4 外观 (次 缺)	导电布、胶带贴附不良	1、ITO 点银浆位置贴附导电布贴偏超出 LCD 边缘 NG 2、导电布未连接上玻璃 NG 3、导电布贴附位置与图纸不符 NG 4、漏贴导电布、IC 防紫外线胶、FPC 保护胶 NG	目视												

1-5 外观 (次缺)	焊接不良 1、A/K 点或 T/P 焊接点歪、锡量超厚、未焊接、虚焊、假焊。 2、A/K 点或 T/P 焊接点未清洁。 3、焊接线沾锡 4、T/P 焊接对位	1、A/K 焊点按搭接面积大于 2/3 OK，焊点厚度不超过工程图上限，A/K 或 TP 焊点未焊接、虚焊、假焊 NG 2、A/K 点或 T/P 焊接点有残渣、松香油、脏污等 NG 3、FPC 焊接线有锡，分开包装，提示入库。 4、以焊接丝印线为基准，下焊超过丝印 0.2mm NG。 上焊与丝印靠齐距离大于 0.5mm NG.	目视 (必要时放大镜检查确认)
1-6 外观 (次缺)	FPC 弯折 1、FPC 边缘未与 BL 边缘平齐，压印线未与定位线对准。 2、元器件顶住背光胶框。	1. FPC 反折要用反折治具检查，未折到位，FPC 边缘须与 BL 边缘平齐，压印线定位孔未对准， NG； 2. 用手指摸背光背面元件区域平整，目视元件有无顶住 BL 边缘，并且预留 0.2MM 间距 OK	卡尺 测量
7.2、电讯检验标准：			
项目	不良描述	判定标准	检验方法
2-1 电讯 (主缺)	漏液晶	LCD 因密封性受损导致空气进入液晶盒内 NG	目视，必要时投低温验证
2-2 电讯 (主缺)	少划： LCD 点亮后有整行(或列)或字段点阵不显的现象	日欣光电 NG 日欣光电 OK	用测架点亮 LCD 后目视

2-3 电讯 (主 缺)	乱讯：在显示字体画面 时有不该显示的地方显 示(画面乱七八糟)	 NG	用测 架点 亮 LCD 后目 视
2-4 电讯 (主 缺)	字节不均(暗画)：需要 显示的字节本身有明暗 不一致现象	 NG	用测 架点 亮 LCD 后目 视
2-5 电讯 (主 缺)	多画：有不需显示之 字节出现在显示区内	 NG	用测 架点 亮 LCD 后目 视
2-6 电讯 (主 缺)	显示深浅：比对样品有 字深字淡现象(在测试 条件一致的情况下量测 产品 Vop 值是否在偏差 范围内)	 深 标准 浅	必要 时可 用主 机板 确认
2-7 电讯 (主 缺)	无显：通电后 LCD 无动 作或无画面	NG	用测 架点 亮 LCD 后目 视

8.模组使用注意事项（Precautions for Use of LCD Modules）

8.1 如果接口定义内有定义 IM0，请根据规格书（4.接口定义）内的定义做正确选择以匹配数据线的位数。

8.2 客户在做结构设计时，请保证机壳开窗尺寸比触摸屏 V.A 单边少 0.3mm。泡棉开窗尺寸比触摸屏 V.A 单边大 0.2mm。

8.3 模组的主要部件 LCD 和 TP 都是由玻璃组成，在测试、使用、移动过程中，请轻拿轻放。当产品不带触摸屏时，靠近 FPC 的屏幕两端绝对不能受力，否则会导致玻璃破损和显示不良的发生。

8.4 粘合偏光片、背光、触摸屏的胶材是有机物质，在接触到甲苯、乙醇、丙酮时，会破坏粘性。在使用中，请防止这些物质接触到产品。

8.5 如果显示表面掉落有灰尘、异物，切忌用手直接擦拭。请用棉签轻轻挑擦。

8.6 如果 LCD 破损导致液晶泄露，请不要让皮肤或衣服沾到液晶。如果不小心碰到，请立即用肥皂和清水清洗。

8.7 用手直接触摸显示区域会造成偏光片的损坏，同时容易引起静电问题。

8.8 当模组运行时，在显示区域施加压力会导致显示不正常。撤去外力，重新开机，可以恢复。

8.9 潮湿的环境可能引起玻璃 ITO 的腐蚀，在使用中，在保证规格书要求的最高温度条件下请确保湿度在 60%以下。